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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,365	TAKEUCHI, MASAHIRO	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-26,40-56,60,61 and 63-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-26,40-56,60,61 and 63-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 63 is objected to because of the following informalities: There is no antecedent basis for the claimed limitation "the first layer" as claimed in claim 63. The phrase "the first layer" should be changed to "the epitaxial layer". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,069,058 to Hong and US Patent No. 6,548,373 to Chuang et al.

Regarding claim 24, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor substrate (110) having a first layer (112);

forming a pad layer (114) on the first layer (112);

forming a polishing stopper layer (116) on the pad layer (114);

forming at least one trench (118a) by etching the first layer (112) while using at least the polishing stopper layer (116) as a mask;

forming a dielectric layer (122) in and above the trench (118a);

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper;

removing the polishing stopper layer (116) after planarizing the dielectric layer (122);

removing the pad layer (114) and exposing the first layer (112) (Li et al. teach the pad oxide layer [114], which is removed in the areas [148]; column 5, lines 26-28. Therefore, the portion of the first layer [112] is exposed) after the moving the polishing stopper layer (116);

forming a sacrificial oxide layer (oxide layer [146]) in direct contact with the first layer (112) (portions of layer [146] is in direct contact with the portions of the first layer [112]; figure 3k) after the removing the pad layer (114).

Li et al. differ from the claimed invention by not showing implanting impurities to form a well in the first layer after the thermally treating the dielectric layer. However, Hong teaches ions implanting to form a well after the thermally treating the dielectric layer (32) (column 2, lines 6-43). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hong into the method taught by Li et al. in order to prevent the diffusion of well into the substrate.

The combined device differs from the claimed invention by not showing thermally treating the dielectric layer after the forming the sacrificial oxide layer. However, Chuang et al. (figures 1 a-c) teach thermally treating the dielectric layer (110) after forming sacrificial oxide layer (103) (column 3, lines 5-44). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chuang et al. into the method taught by Li et al. and Hong in order to reduce the stress of the dielectric layer.

The combined device differs from the claimed invention by not showing thermally treating the dielectric layer at a temperature of at least about 1050° C after the forming the sacrificial oxide layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally treating the dielectric layer to a thermal treatment at a temperature of at least 1050° C in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 20, the combined device shows the first layer (Li et al.; 112) comprises an epitaxial growth layer.

Regarding claim 21, the combined device shows removing the polishing stopper layer (Li et al.; 116) after planarizing the dielectric layer (Li et al.; 122).

Regarding claim 22, the combined device shows an oxidizing at least a portion of the first layer (Li et al.; 112) in the at least one trench prior to forming the dielectric layer in and above the trench.

Regarding claim 23, the combined device shows forming a pad layer (Li et al.; 114) between the first layer (Li et al.; 112) and the polishing stopper layer (Li et al.; 116).

Regarding claim 25, the combined device differs from the claimed invention by not showing the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen in order to

increase the density of the dielectric layer. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Hong in view of Chuang et al., and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 26, the disclosures of Li et al., Hong and Chuang et al. are discussed as applied to claims 20-25 above.

The combined device differs from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al., Hong and Chuang et al. in order to improve the dielectric property of the dielectric layer.

4. Claims 40-42, 47-49 and 51-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,087,243 to Wang and US Patent No. 6,221,735 to Manley et al.

Regarding claim 40, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a polishing stopper layer (116) on a semiconductor layer (112);

forming an opening in the polishing stopper layer (116) and a trench (118a) in the semiconductor layer (110);

forming a dielectric layer (122) in the trench, in the opening in the stopper layer (116), and on the stopper layer;

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper; and

removing the polishing stopper layer (116) after the planarizing the dielectric layer (122);

Li et al. differ from the claimed invention by not showing conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer. However, Wang teaches conducting a thermal treatment of the dielectric layer (16) after removing the polishing stopper layer (polishing stopper layer [nitride layer 13] is removed and then heating the oxide trench [16]) (column 6, lines 44-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wang into the method taught by Li et al. in order to increase the density of the dielectric layer.

The combined device differs from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted at a temperature of at least 1050° C in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The combined device differs from the claimed invention by not showing after the thermal treatment of the dielectric layer, performing a first implanting operation into the semiconductor including implanting impurity ions into the semiconductor layer. However, Manley et al. teach implanting ions into the substrate after the annealing step of the dielectric layer (column 3, lines 47-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Manley et al. into the method taught by Li et al. and Wang in order to prevent the diffusion of the implanting ions.

Regarding claim 41, the combined device shows forming a pad layer (Li et al.; 114) on the semiconductor layer (Li et al.; 112) prior to form the polishing stopper layer (Li et al.; 116), wherein the pad layer is formed between and in direct contact with the semiconductor layer and the polishing stopper layer.

Regarding claim 42, the combined device shows the opening in the polishing stopper layer (Li et al.; 116) also extends through the pad layer (Li et al.; 114).

Regarding claim 47, the combined device differs from the claimed invention by not showing the dielectric layer is formed with a film density of at lest 2.1 g/cm^3. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at least 2.1 g/cm^3 in order to provide a good gap-fill characteristic. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 48, the combined device differs from the claimed invention by not showing the temperature of the thermal treatment is 1100° C or higher. It would have been

obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is 1100° C or higher in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 49, the combined device differs from the claimed invention by not showing the temperature of the thermal treatment is in the range 1050° C to 1250° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is in the range 1050° C to 1250° C in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 51, the combined device shows the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer (Li et al.; 120) thereon, wherein the dielectric layer (Li et al.; 122) is formed in direct contact with the thermal oxide layer (Li et al.; 120).

Regarding claim 52, the combined device differs from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a

temperature in the range of at 700° C to 1150° C in order to reduce the stress of the dielectric layer in the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 53, the combined device differs from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 950° C to 1150° C in order to reduce the stress of the dielectric layer in the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 54, the combined device differs from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm in order to prevent the diffusion of other layer to the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 55, the combined device shows the semiconductor layer (Li et al.; 112) comprises an epitaxial growth layer formed on a semiconductor substrate (Li et al.; 110).

Regarding claim 56, the combined device differs from the claimed invention by not showing the trench is formed with a trench width of no greater than 0.35 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the trench is formed with a trench width of no greater than 0.35 micrometer in order to reduce the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Wang in view of Manley et al., and further in view of US Patent No. 6,258,692 to Chu et al. and US Patent No. 6,265,269 to Chen et al.

Regarding claim 43, the disclosures of Li et al., Wang and Manley et al. are discussed as applied to claims 40-42, 47-49 and 51-56 above.

Li et al. differ from the claimed invention by not showing isotropically etching the pad layer. However, Chu et al. teach the pad oxide layer (202a), which is removed (etched) by isotropic etching (column 4, lines 36-37). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chu et al. into the method taught by Li et al. in order to create a smooth etching surface of the pad oxide layer.

Li et al. differ from the claimed invention by not showing isotropically etching upper portions of the dielectric layer. However, Chen et al. teach the dielectric layer (30; remaining on the upper portion of the trench), which is removed (etched) by isotropic etching (column 3, lines 46-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen et al. into the method taught by Li et al. in order to create a smooth etching surface of the dielectric layer. The combined device shows isotropically etching the pad layer and upper portions of the dielectric layer after the removing the polishing stopper layer and prior to the conducting the thermal treatment.

6. Claims 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,087,243 to Wang, US Patent No. 6,069,058 to Hong, US Patent No. 6,258,692 to Chu et al. and US Patent No. 6,265,269 to Chen et al.

Regarding claim 44, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a polishing stopper layer (116) on a semiconductor layer (112);

forming an opening in the polishing stopper layer (116) and a trench (118a) in the semiconductor layer (110);

forming a pad layer (114) on the semiconductor layer (112) prior to forming the polishing stopper layer (116), wherein the pad layer (114) is formed between and in direct contact with the semiconductor layer (112) and the polishing stopper layer (116), and wherein the opening in the polishing stopper layer (116) also extends through the pad layer (114);

forming a dielectric layer (122) in the trench, in the opening in the stopper layer (116), and on the stopper layer;

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper; and

removing the polishing stopper layer (116) after the planarizing the dielectric layer (122).

Li et al. differ from the claimed invention by not showing conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer. However, Wang teaches conducting a thermal treatment of the dielectric layer (16) after removing the polishing stopper layer (polishing stopper layer [nitride layer 13] is removed and then heating the oxide trench [16]) (column 6, lines 44-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wang into the method taught by Li et al. in order to increase the density of the dielectric layer.

The combined device differs from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted at a temperature of at least 1050° C in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The combined device differs from the claimed invention by not showing forming a well in the semiconductor layer after the thermally treating of the dielectric layer. However, Hong teaches ions implanting to form a well after the thermally treating the dielectric layer (32)

(column 2, lines 6-43). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hong into the method taught by Li et al. and Wang in order to prevent the diffusion of well into the substrate.

Li et al. differ from the claimed invention by not showing isotropically etching the pad layer. However, Chu et al. teach the pad oxide layer (202a), which is removed by isotropic etching (column 4, lines 36-37). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chu et al. into the method taught by Li et al. in order to create a smooth etching surface of the pad oxide layer.

Li et al. differ from the claimed invention by not showing isotropically etching upper portions of the dielectric layer. However, Chen et al. teach the dielectric layer (30; remaining on the upper portion of the trench), which is removed by isotropic etching (column 3, lines 46-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen et al. into the method taught by Li et al. in order to create a smooth etching surface of the dielectric layer.

Regarding claim 45, the combined device further shows an oxide layer (Li et al.; 122) is formed on the exposed upper surfaces of the semiconductor layer (Li et al.; 112) after the isotropically etching and prior to the forming a well in the semiconductor layer.

Regarding claim 46, the combined device shows the oxide layer (Li et al.; 122) is formed prior to the conducting a thermal treatment of the dielectric layer.

7. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Wang in view of Manley et al., and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 50, the disclosures of Li et al., Wang and Manley et al. are discussed as applied to claims 40-42, 47-49 and 51-56 above.

The combined device differs from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al., Wang and Manley et al. because it improves the dielectric property of the dielectric layer.

8. Claims 60 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,069,058 to Hong.

Regarding claim 60, Li et al. (figures 3a-m) teaches a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor layer (112);

forming a pad oxide layer (114) on the semiconductor layer (112);

forming a polishing stopper layer (116) in direct contact with the pad oxide layer (114), wherein the pad oxide layer (114) is positioned between the semiconductor layer (112) and the polishing spotter layer (116);

forming a patterned resist layer on the polishing stopper layer (116), the patterned resist layer including an open region exposing part of the polishing stopper layer (116) over a trench formation region;

using the patterned resist layer as a mask, etching the polishing stopper layer (116) and the pad oxide layer (114) so that a portion of the semiconductor layer (112) is exposed; after the etching the polishing stopper layer (116) removing the patterned resist layer;

after the removing the patterned resist layer, etching the semiconductor layer (112) to form at least one trench therein, using the polishing stopper layer (116) as a mask;

forming a dielectric layer (122) in and above the at least one trench;

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper; and

removing the polishing stopper layer (116) and the pad oxide layer (114) so that an upper surface of the semiconductor layer (112) is exposed (the polishing stopper layer [116] is removed; figure 3g; and the pad oxide layer [114], which is removed in the areas [148]; figure 3k; column 5, lines 26-28. Therefore, the portion of the first layer [112] is exposed).

Li et al. differ from the claimed invention by not showing heating the dielectric layer after the removing the polishing stopper layer and the pad oxide. However, Hong (figures 1-12) teaches removing the portion of the polishing stopper layer (24) and the pad oxide (22) (figure 4) and heating the dielectric layer (32) (column 2, lines 30-38) (figure 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hong into the method taught by Li et al. in order to increase the density of the dielectric layer.

Li et al. and Hong differ from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted

at a temperature of at least 1050° C in order to increase the density of the dielectric layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Li et al. differ from the claimed invention by not showing forming a well in the semiconductor layer after the thermally treating of the dielectric layer. However, Hong teaches ions implanting to form a well after the thermally treating the dielectric layer (32) (column 2, lines 6-43). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hong into the method taught by Li et al. in order to prevent the diffusion of well into the substrate.

Regarding claim 61, the combined device shows after forming the at least one trench and prior to form the dielectric layer (Li et al.; 122), forming a thermal oxide layer (Li et al.; 120) on the semiconductor substrate (Li et al.; 110) in the at least one trench.

9. Claims 63-65 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,548,373 to Chuang et al. and US Patent No. 6,221,735 to Manley et al.

Regarding claim 63, Li et al. (figures 3a-m) teach method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor substrate (110) having an epitaxial layer (112) thereon ;

forming a pad layer (114) on the epitaxial layer (112);

forming a polishing stopper layer (116) on the pad layer (114);

forming at least one trench (118a) by etching the epitaxial layer (112) while using at least the polishing stopper layer (116) as a mask;

forming a dielectric layer (122) in and above the at least one trench (118a);

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper;

etching the polishing stopper layer (116) after planarizing the dielectric layer (122);

etching the pad layer (114) and exposing the epitaxial layer (112) (Li et al. teach the pad oxide layer [114], which is removed (etched) in the areas [148]; figure 3k; column 5, lines 26-28. Therefore, the portions of the first layer [112] are exposed), after the etching the polishing stopper layer (116);

forming a sacrificial oxide layer (146) on the exposed epitaxial layer (112), after the removing the pad layer (114).

Li et al. differ from the claimed invention by not showing thermally treating the dielectric layer after the forming the sacrificial oxide layer. However, Chuang et al. (figures 1 a-c) teach thermally treating the dielectric layer (110) after forming sacrificial oxide layer (103) (column 3, lines 5-44). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chuang et al. into the method taught by Li et al. in order to increase the density of the dielectric layer.

The combined device differs from the claimed invention by not showing thermally treating the dielectric layer at a temperature of at least about 1050° C after the forming the sacrificial oxide layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally treating the dielectric layer to a thermal treatment at a temperature of at least 1050° C in order to increase the density of the dielectric layer.

Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The combined device differs from the claimed invention by not showing after the thermal treatment of the dielectric layer, implanting impurity ions in the epitaxial layer. However, Manley et al. teach implanting ions after the annealing step of the dielectric layer (column 3, lines 47-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Manley et al. into the method taught by Li et al., Chuang et al. in order to prevent the diffusion of the implanting ions. The combined device shows implanting impurity ions in the epitaxial layer after the thermally treating the dielectric layer and after the implanting impurity ions, removing the sacrificial oxide layer (a portion of layer [146] is removed as shown in figure 3l; a opening [152]).

Regarding claim 64, the combined device shows forming a thermal oxide layer (Li et al.; 120) in the at least one trench (Li et al.; 118a) prior to the forming a dielectric layer (122) in and above the at least one trench (Li et al.; 118a).

Regarding claim 65, the combined device differs from the claimed invention by not showing the dielectric layer is formed with a film density of at lest 2.1 g/cm^3. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at least 2.1 g/cm^3 in order to provide a good gap-fill characteristic. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 67, the combined device differs from the clamed invention by not showing the epitaxial growth layer has a thickness of at least 2 μm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the epitaxial growth layer has a thickness of at least 2 μm in order to provide high quality silicon to form device in the substrate. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

10. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Chuang et al. in view of Manley et al., and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 66, the disclosures of Li et al., Chuang et al. and Manley et al. are discussed as applied to claims 63-65 and 67 above

The combined device differs from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al., Hong and Chuang et al. in order to improve the dielectric property of the dielectric layer.

Response to Arguments

Applicant's arguments filed 09/27/04 have been fully considered but they are not persuasive.

It is argued, in page 10 of the remarks, that Li et al., Horita et al. and Chuang et al. do not teach or suggest exposing the first layer and forming a sacrificial oxide layer in direct contact with the first layer. This argument is not convincing because the combined device (Li et al., Hong and Chuang et al.) shows removing the pad layer (114) and exposing the first layer (112) (Li et al. teach the pad oxide layer [114], which is removed in the areas [148]; figure 3k; column 5, lines 26-28. Therefore, the portion of the first layer [112] is exposed); and forming a sacrificial oxide layer (146) in direct contact with the first layer (112) (portions of layer [146] is in direct contact with the portions of the first layer [112]; figure 3k).

It is argued, in page 12 of the remarks, that Li et al., Wang and Horita et al. do not teach or suggest isotropically etching the pad layer and upper portions of the dielectric layer. This argument is not convincing because the combined device (Li et al., Wang, Hong, Chu et al. and Chen et al.) shows isotropically etching the pad layer and upper portions of the dielectric layer for the reasons that are discussed above.

It is argued, in page 13 of the remarks, that Li et al., Wang and Horita do not teach or suggest removing the polishing stopper and the pad oxide layer so that an upper surface of the semiconductor layer is exposed and heating the dielectric layer after the removing the polishing stopper layer and the pad oxide layer. This argument is not convincing because the combined device (Li et al. and Hong) shows the removing the polishing stopper and the pad oxide layer so that an upper surface of the semiconductor layer is exposed and heating the dielectric layer after

the removing the polishing stopper layer and the pad oxide layer for the reasons that are discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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qv
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